WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a plurality of flip-flops;

a plurality of stages of clock drivers including ith ($1 \leqq i \leqq n$) stages to feed clock signals to the plurality of flip-flops; and

a plurality of clock lines including ith ($2 \leqq i \leqq n$) clock lines to connect between a clock driver of an (i-1) th stage and clock drivers of an ith stage and (n+1) th clock lines to connect between a clock driver of an nth stage and the plurality of flip-flops,

wherein differences between a maximum length and a minimum length of the ith clock lines are smaller than differences between a maximum length and a minimum length of the (n+1) th clock lines.

2. The semiconductor integrated circuit device according to claim 1, wherein the ith clock lines are equalized in length and the (n+1) th clock lines have a shortest possible length.

3. The semiconductor integrated circuit device according to claim 1, further comprising:

a clock generator to generate clock signals having different phases,

wherein plural clock drivers are provided for the first stage and first clock lines are provided to connect between the clock generator and the plural clock drivers of first stage, and

wherein the plural clock drivers of the first stage are provided respectively for the clock signals having different phases.

4. The semiconductor integrated circuit device according to claim 3, wherein the clock generator is placed in a peripheral area of a chip and the plural clock drivers of first stage are placed in a center area of the chip.

5. The semiconductor integrated circuit device according to claim 3, further comprising:

a circuit including the plurality of flip-flops; and

a plurality of power lines to apply a supply voltage to the circuit,

wherein clock drivers of the first stage are provided adjacent to different ones of said power lines.

6. The semiconductor integrated circuit device according to claim 1,

wherein one of the ith clock lines has a first junction point, and

wherein a width of the ith clock lines between a clock driver of the first stage and the first junction point is larger than a width of the ith clock line between the first junction point and clock driver of the second stage.

7. The semiconductor integrated circuit device according to claim 1,

wherein a third clock line has a second junction point, and

wherein a width of the third clock line between a clock driver of the second stage and the second junction point is larger than a width of the third clock line between the second junction point and a clock driver of the third stage.

8. A semiconductor integrated device comprising:

a plurality of circuit blocks including at least a data pass and I/O circuit;

a plurality of flip-flops included in the plurality of circuit blocks;

a plurality of stages of clock drivers including an ith ($1 \leqq i \leqq n$) stage to feed clock signals to the plurality of flip-flops; and

a plurality of clock lines including ith ($2 \leqq i \leqq n$) clock lines to connect between a clock driver of an (i-1) th stage and clock drivers of an ith stage and (n+1) th clock lines to connect between a clock driver of an nth stage and the plurality of flip-flops,

wherein differences between a maximum length and a minimum length of the ith clock lines are smaller than differences between a maximum length and a minimum length of the (n+1) th clock lines.

9. The semiconductor integrated circuit device according to claim 8, further comprising:

a first area to provide clock drivers of nth and (n-1) th stages to feed clock signals to flip-flops of the data path,

wherein the first area is adjacent to an area where the data pass is provided.

10. The semiconductor integrated circuit device according to claim 8, further comprising:

a power line to apply a supply voltage to the circuit blocks,

wherein the first area is adjacent to the power lines.

11. The semiconductor integrated circuit device according to claim 8, further comprising:

a second area to provide clock drivers of nth and (n-1) th stages to feed clock signals to flip-flops of the I/O circuit;

wherein the second area is adjacent to an area where the I/O circuit is provided.